Performance Specification

ITEM		Ex1s	Ex1n, Ex2n
Operating control method		Cyclic operation by stored program	
I/O control method		Batch processing method (when END instruction is executed)	
Operation time		Basic instruction 0.5us, Applied instruction from 2us to several 100us.	
Programming language		Relay symbolic language + Step ladder	
Program capacity / memory		2000 steps (built in EEprom)	8000 steps (built in EEprom)
Number of instruction		Basic instruction: 27; Step ladder instruction: 2; Applied instruction: 105(1s) 107(1n) 118(2n)	
Input Relay		1s : X00 ~ X17 1n : X000 ~ X177 (Sink/Source DC24V 7mA photo coupler isolation)	
Output Relay		1s : Y00 ~ Y17 1n : Y000 ~ Y177 (Relay : AC250V/1A or Transistor : DC30V/0.5A)	
Auxiliary Relay (M)	Latched	M000 ~ M499 (EEprom backup)	
	General	M500 ~ M1535 (no backup)	
	Special	M8000 ~ M8255 (no backup)	
State Relay (S)	Latched	S000 ~ S499 (EEprom backup)	
	General	S500 ~ S999 (no backup)	
Timer (T)	100 msec	T000 ~ T199 (no backup)	
	10 msec	T200 ~ T245 (no backup)	
	1 ms integration	4 points, T246 ~ T249 (EEprom backup)	
	100 ms integration	6 points, T250 ~ T255 (EEprom backup)	
	Analog	2 points, (Define by user)	
Counter (C)	16bits Counter	C00 ~ C31 Latched (EEprom backup)	
		C32 ~ C199 General	
	32bits Counter	C200 ~ C215 General	
		C216 ~ C255 Latched (backup)	
	High Speed Counter	6 points : X0 ~ X5 ; X0 or X1 for 1 phase 60KHz , X2 ~ X5 for 1phase 10KHz	
		X0 and X1 for 2 phase 30KHz , X2 ~ X5 for 2phase 5KHz	
Data Register	Latched	D000 ~ D255 (EEprom backup)	
	General	D256 ~ D3999 (can use FNC(12) MOV stored at EEPROM)	
	Special	D8000 ~ D8255 (no backup)	
Index		V0 ~ V7, Z0 ~ Z7	
Nest Routine (N)		N0 ~ N7	
Subroutine Pointer (P)		P000 ~ P127 (CJ, CALL)	
Interrupt Pointer (I)		I00x, I10x, I20x, I30x, I40x, I50x (External interrupt), x=1 rising edge, x=0 falling edge	
		I6xx, I7xx, I8xx (Timer interrupt), xx=10~99ms	
		I010, I020, I030, I040, I050, I060 : High speed counter interrupt	
Communication Interface		RS-232C (COM1) & RS-232C/RS-422,RS-485 (COM2)	
Calendar (Option)		Week, Year, Month, Day, Hour, Minute, Second	
Constant(K)	Decimal	16 bits: -32,768 ~ +32,767	
		32 bits: -2,147,483,648 ~ +2,147,483,647	
Constant(H)	Hexadecimal	16 bits: 0000 ~ FFFF	
		32 bits: 00000000 ~ FFFFFFFF	

@ Basic Instruction

Mnemonic	Function	Devices	Mnemonic	Function	Devices
LD	LoaD	X . Y. M . S . T . C	MC	Master Control	Y . M .
LD I	LoaD Inverse	X . Y. M . S . T . C	MCR	Master Control Reset	N/A
OUT	OUT	Y. M . S . T . C	MPS	Point Store	N/A
AND	AND	X . Y. M . S . T . C	MRD	Read	N/A
AN I	AND Inverse	X . Y. M . S . T . C	MPP	PoP	N/A
OR	OR	X . Y. M . S . T . C	END	END	N/A
OR I	OR Inverse	X . Y. M . S . T . C	LDP	LoaD Pulse	X . Y. M . S . T . C
ANB	ANd Block	N/A	LDF	LoaD Falling pulse	X . Y. M . S . T . C
ORB	OR Block	N/A	ANP	ANd Pulse	X . Y. M . S . T . C
NOP	No Operation	N/A	ANF	ANd Falling pulse	X . Y. M . S . T . C
SET	SET	Y . M . S	ORP	OR Pulse	X . Y. M . S . T . C
RST	ReSeT	X . Y . M . S . T . C	ORF	OR Falling pulse	X . Y. M . S . T . C
PLS	PuLSe	Y . M .	I NV	INVerse	N/A
PLF	PuLse Falling	Y . M .			

@ STL Instruction

Mnemonic	Function	Devices	Mnemonic	Function	Devices
STL	Beginning of stage Ladder	S	RET	End of Stage Ladder	N/A

@ Applied Instruction

FNC NO.	Mnemonic	(D)	(P)	Function	Ex1s	Ex1n	Ex2n	FNC NO	Mnemonic	(D)	(P)	Function	Ex1s	Ex1n	Ex2n
0	CJ		B	Conditional Jump	B	B	B	74	SEGL			Seven segment with latch			
1	CALL		B	Call subroutine	B	B	B	75	ARWS			Arrow switch			
2	SRET			Subroutine return	B	B	B	76	ASC			ASCII code conversion	B	B	B
3	I RET			Interrupt return	B	B	B	77	PR			Print			
4	E I			Enable interrupts	B	B	B	78	FROM	B	B	FROM		B	B
5	D I			Disable interrupts	B	B	B	79	TO	B	B	TO		B	B
6	FEND			First end	B	B	B	80	RS			Serial Communications instruction	B	B	B
7	WDT		B	Watch dog timer refresh	B	B	B	81	PRUN	B	B	Parallel run	B	B	B
8	FOR			Start of a FOR-NEXT loop	B	B	B	82	ASCI		B	Converts HEX to ASCII	B	B	B
9	NEXT			End of a FOR-NEXT loop	B	B	B	83	HEX		B	Converts ASCII to HEX	B	B	B
10	CMP	B	B	Compare	B	B	B	84	CCD		B	Check Code	B	B	B
11	ZCP	B	B	Zone compare	B	B	B	85	VRRD		B	Volume read	B	B	B
12	MOV	B	B	Move	B	B	B	86	VRSC		B	Volume scale	B	B	B
13	SMOV		B					88	P I D			PID control loop register each	B	B	B
14	CML	B	B	Compliment	B	B	B								
15	BMOV		B	Block move	B	B	B	110	ECMP	B	B	Floating Point Compare			B
16	FMOV	B	B	Fill move	B	B	B	111	EZCP	B	B	Floating Point Zone Compare			B
17	XCH	B	B	Exchange	B	B	B	118	EBCD	B	B	Float to Scientific conversion			
18	BCD	B	B	B I N → BCD Binary coded decimal	B	B	B	119	EBIN	B	B	Scientific to Float conversion			
19	B I N	B	B	BCD → B I N Binary	B	B	B	120	EADD	B	B	Floating Point Addition			B
20	ADD	B	B	Addition (S1) + (S2) → (D)	B	B	B	121	ESUB	B	B	Floating Point Sub-traction			B
21	SUB	B	B	Subtract (S1) – (S2) → (D)	B	B	B	122	EMUL	B	B	Floating Point Multiplication			B
22	MUL	B	B	Multiplication (S1) × (S2) → (D)….(D)	B	B	B	123	EDIV	B	B	Floating Point Division			B
23	DIV	B	B	Division (S1) ÷ (S2) → (D)….(D)	B	B	B	127	ESQR	B	B	Floating Point Square Root			B
24	I NC	B	B	Increment (D)+1 → (D)	B	B	B	129	INT	B	B	Float to Integer			B
25	DEC	B	B	Decrement (D) -1 → (D)	B	B	B	130	SIN	B	B	Sine			B
26	WAND	B	B	Logical word AND (S1) AND (S2) → (D)	B	B	B	131	COS	B	B	Cosine			B
27	WOR	B	B	Logical word OR (S1) OR (S2) → (D)	B	B	B	132	TAN	B	B	Tangent			B
28	WXOR	B	B	Logical exclusive OR (S1)⊻(S2) → (D)	B	B	B	147	SWAP	B	B	Byte Swap	B	B	B
29	NEG	B	B	Negation /(D) +1 → (D)	B	B	B	155	ABS	B		Absolute current value read			
30	ROR	B	B	Rotation Right	B	B	B	156	ZRN	B		Zero return	B	B	B
31	ROL	B	B	Rotation Left	B	B	B	157	PLSV	B		Pulse V	B	B	B
32	RCR	B	B	Rotation Right with Carry	B	B	B	158	DRV I	B		Drive to increment	B	B	B
33	RCL	B	B	Rotation Left with Carry	B	B	B	159	DRVA	B		Drive to absolute	B	B	B
34	SFTR		B	Bit Shift Right	B	B	B	160	TCMP		B	Time Compare	B	B	B
35	SFTL		B	Bit Shift Left	B	B	B	161	TZCP		B	Time Zone Compare	B	B	B
36	WSFR		B	Word Shift Right	B	B	B	162	TADD		B	Time Addition	B	B	B
37	WSFL		B	Word Shift Left	B	B	B	163	TSUB		B	Time Subtraction	B	B	B
38	SFWR		B	Shift Register Write	B	B	B	166	TRD		B	Time Read	B	B	B
39	SFRD		B	Shift Register Read	B	B	B	167	TWR		B	Time Write	B	B	B
40	ZRST		B	Zone Reset	B	B	B	169	HOUR	B		Hour meter			
41	DECO		B	Decode	B	B	B	170	GRY	B	B	Gray Code	B	B	B
42	ENCO		B	Encode	B	B	B	171	GBIN	B	B	Gray Code	B	B	B
43	SUM	B	B	The Sum of Active Bits	B	B	B	176	RD3A		B	Read EX-3A			
44	BON	B	B	Check Specified Bit Status	B	B	B	177	WR3A		B	Write EX-3A			
45	MEAN		B	Mean	B	B	B	224	LD=	B		Load compare when (S1) = (S2) ON	B	B	B
46	ANS			Timed annunciator Set				225	LD>	B		Load compare when (S1) > (S2) ON	B	B	B
47	ANR		B	Annunciator Reset				226	LD<	B		Load compare when (S1) < (S2) ON	B	B	B
48	SQR	B	B	Square Root	B	B	B	228	LD<>	B		Load compare when (S1)<>(S2) ON	B	B	B
49	FLT	B	B	Floating Point	B	B	B	229	LD ↑	B		Load compare when (S1) ↑(S2) ON	B	B	B
50	REF		B	Refresh	B	B	B	230	LD ↓	B		Load compare when (S1) ↓ (S2) ON	B	B	B
51	REFF		B	Refresh and filter adjust	B	B	B	232	AND=	B		AND compare when (S1) = (S2) ON	B	B	B
52	MTR			Input matrix	B	B	B	233	AND>	B		AND compare when (S1) > (S2) ON	B	B	B
53	HSCS	B		High speed counter set	B	B	B	234	AND<	B		AND compare when (S1) < (S2) ON	B	B	B
54	HSCR	B		High speed counter reset	B	B	B	236	AND<>	B		AND compare when (S1)<>(S2) ON	B	B	B
55	HSZ	B		High speed counter zone compare	B	B	B	237	AND ↑	B		AND compare when (S1) ↑(S2) ON	B	B	B
56	SPD			Speed detect	B	B	B	238	AND ↓	B		AND compare when (S1) ↓ (S2) ON	B	B	B
57	PLSY	B		Pulse Y output	B	B	B	240	OR=	B		OR compare when (S1) = (S2) ON	B	B	B
58	PWM			Pulse width modulation	B	B	B	241	OR>	B		OR compare when (S1) > (S2) ON	B	B	B
59	PLSR	B		Ramp Pulse output	B	B	B	242	OR<	B		OR compare when (S1) < (S2) ON	B	B	B
60	I ST			Initial State				244	OR<>	B		OR compare when (S1)<>(S2) ON	B	B	B
61	SER	B	B	Search a Data Stack				245	OR ↑	B		OR compare when (S1) ↑(S2) ON	B	B	B
62	ABSD	B		Absolute drum sequencer	B	B	B	246	OR ↓	B		OR compare when (S1) ↓ (S2) ON	B	B	B
63	I NCD			Incremental drum sequencer	B	B	B								
64	TTMR			Teaching timer											
65	STMR			Special timer											
66	ALT		B	Alternate state	B	B	B								
67	RAMP			Ramp variable value	B	B	B								
68	ROTC			Rotary table control											
69	SORT			SORT Tabulated Data											
70	TKY	B		Ten key input	B	B	B								
71	HKY	B		Hexadecimal key input	B	B	B								
72	DSW			Digital switch	B	B	B								
73	SEGD		B	Seven segment decoder	B	B	B								